input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line.

8. (Amended) The circuit of claim 1, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

9. (Twice Amended) The circuit of claim 8, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signals;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said inputs, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second, complementary internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

11. (Amended) The circuit of claim 1, further comprising a first and second driver circuit, said first and second driver circuit connected to said first and second complementary clock signal input/output lines, respectively.

14. (Amended) The circuit of claim 1, wherein each of said first and second inverters are comprised of series connected complimentary transistors, the respective connection terminal of said series connected complimentary transistors being coupled to a respective one of said complementary clock signal input/output lines.

15. (Amended) The circuit of claim 14, wherein said first and second inverters include:

a first N-channel transistor coupled to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

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said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor.

16. (Amended) A circuit for reducing clock signal skew comprising:

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at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second internal complementary clock signals;

a first N-channel transistor coupled to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor.

20. (Amended) The circuit of claim 16, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

21. (Twice Amended) The circuit of claim 20, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

23. (Amended) The circuit of claim 16, further comprising a first and second driver circuit, said first and second driver circuit connected to said first and second complementary clock signal input/output lines, respectively.

26. (Amended) A circuit for reducing signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second, complementary clock signal input/output line; and

a first and second driver circuit, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

33. (Amended) The circuit of claim 26, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

34. (Twice Amended) The circuit of claim 33, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

87. (Amended) The method of claim 82, wherein said act of receiving first and second external clock signals is performed in connection with the operation of a random access memory.